**CMPE 344 Term Project**

**Due: January 24th, 2021**

The topic of your term project is examination of the processor you have been assigned. Please examine it in terms of:

1. Its general architecture: Is it RISC or CISC? If it is RISC, you will compare it with ARM Cortex-A8, discussed in the book. If it is CISC, compare it with Intel Core i7 920 Nehalem discussed in the book. Describe its general characteristics, its semiconductor technology, clock rate, etc.
2. Its instruction set: examine its assembly briefly. What kind of operations does it have, such as basic arithmetic, floating point, vector? What kind of addressing modes does it have? What kind of registers does it have?
3. Its pipeline: Try to find the block diagram. How many stages? What are the pipeline stages? Is control hardwired or microcoded? Number of functional units? Is it multiple issue? Static or dynamic? Does it support out-of-order speculation? Branch speculation? Load speculation?
4. Its memory structure: caches, TLB. How many levels? For each one, whether associative or direct mapped? Write through or write back? Does it have a write buffer and if yes, what is the size? Does it use write allocate, or write around?
5. Parallelism: How many cores? How many threads per core? How fast is it in terms of benchmarks (CPI, GFLOPS, other metrics)?

After filling in the summary table below, discuss each of the above issues in separate sections with pictures, block diagrams, etc. As conclusion, discuss issues such as where this processor has been used (embedded, automotive, phones, PCs, servers?), commercial success (how many units have been sold); whether there were problems (issues requiring recall, firmware update or patching); if yes, how have they been solved? Other business issues of interest may also be mentioned.

Be sure not to do cut and paste (this is plagiarism; you cannot use other sources text directly, even if you cite them). Cite all your references and list them in the references section. You will submit your term paper as a Turnitin assignment. This software checks your paper against all sources as well as your classmates’ papers and detects common text as well as figures and tables. However, in this assignment, figures can be copied from original source, which must be cited. The table below will also be similar in everyone; so it will not be checked for similarity. You may submit once and see your similarity score; and correct and submit again.

|  |  |  |
| --- | --- | --- |
|  | **Your assigned processor** | **Core i7 920** or **ARM Cortex A8** |
| **GENERAL** | | |
| Designed by (company) | Intel | Intel |
| Produced by (company) | Intel | Intel |
| Year | April 2020 | November 2008 |
| Clock rate | 3.7 GHz | 2.67 GHz |
| **SEMICONDUCTOR TECHNOLOGY** | | |
| #transistors | Unknown**\*** | 731 million |
| #cores/chip | 10 | 4 |
| power consumption | 125 W | 130 W |
| #units sold to date |  |  |
| Type: RISC/CISC/GPU | CISC | CISC |
| **ASSEMBLY LANG** | | |
| # instructions |  |  |
| Instruction types (basic, floating point, vector, etc.) |  | Floating points |
| # registers |  |  |
| word size |  |  |
| # addressing modes |  |  |
| **PIPELINE** | | |
| # pipeline stages | 14 | 14 |
| # functional units |  | 6 |
| multiple issue (Yes/No)  dynamic/static | Yes, dynamic | Yes, dynamic |
| pipeline control: hardwired/microprogrammed | microprogrammed | microprogrammed |
| Out-of-Order speculation (Yes/No) | Yes | Yes |
| Branch speculation (Yes/No) | Yes | Yes |
| Load speculation (Yes/No) | No | No |
| **MEMORY** | | |
| # Levels of cache | 3 | 3 |
| L1 cache (Inst/Data) size | 32 KiB each for instructions/data per core | 32 KiB each for instructions/data per core |
| L1 cache (Inst/Data) block size | 64 bytes | 64 bytes |
| L1 cache (Inst/Data) mechanism (direct mapped/assoc./set assoc.) | 8 way (I), 8 way(D) set associative | 4 way (I), 8 way(D) set associative |
| L1 cache write mechanism | Write back | Write back,  No-write-allocate |
| L1 replacement policy | Approximately LRU | Approximately LRU |
| L1 cache hit time (# cycles) | 32 clock cycles | 4 clock cycles |
| L2 cache (Inst/Data) size | 256 KiB | 256 KiB |
| L2 cache (Inst/Data) block size | 64 bytes | 64 bytes |
| L2 cache (Inst/Data) mechanism (direct mapped/assoc./set assoc.) | 8 way set associative | 8 way associative |
| L2 cache write mechanism | Write back | Write back |
| L2 replacement policy | Approximately LRU | Approximately LRU |
| L2 cache hit time (# cycles) | 64 clock cycles | 10 clock cycles |
| L3 cache (Inst/Data) size | 20 MiB | 8 MiB |
| L3 cache (Inst/Data) block size | 64 bytes | 64 bytes |
| L3 cache (Inst/Data) mechanism (direct mapped/assoc./set assoc.) | 16 way set associative | 16 way set associative |
| L3 cache write mechanism | Write back | Write back,  Write alloccate |
| L3 replacement policy | Approximately LRU | Approximately LRU |
| L3 cache hit time (# cycles) | 32 clock cycles | 35 clock cycles |
| TLB levels, organization | 1 TLB for instructions and 1 TLB for data per core | 1 TLB for instructions and 1 TLB for data per core |
| physical address space |  | 44 bits |
| virtual address space |  | 48 bits |
| page size |  | Variable 4 KiB, 2/4 MiB |
| **OTHER ISSUES** | | |
| Benchmarks | %101 | %64.7 |
| CPI in benchmarks, etc. |  |  |
|  |  |  |